

Superconducting TES Array Electronics Block Diagrams

Definition document draft - version 1 May 20, 2002 - Dominic Benford

The array block diagrams in this document consist of a variety of setups for operating Nx32 detectors.

It is assumed that the final arrays require 32 pairs for addressing (derived from a cryogenic address driver). This requires a single 65-pin nanonics connector with no termination anywhere unless it is added onto the detector package itself to better match the impedance of the twisted pairs.

It is further assumed that each column requires 1st FB, Detector Bias, and 2nd FB to be wired to the package. The package must have each column's 2nd Out wired to the SA housing. The SA housing will require a 3rd FB and 3rd Out to connect to the RT electronics.

I have made the choice to wire the 2nd Bias to the SA housing, which has a few benefits:

- requires fewer wires to the cold stage
- doesn't put a load resistor on the cold stage
- permits the flex-to-nanonics boards to be in units of 3 flex lines for both the SA and the Detector wiring.

For the test package (2x32), it is assumed that we will have two different packages with the same connector layout.

- One package will be set up exactly as a 2x32 mux, with an extra detector bias per column.
- One package will be set up to run 4 devices straight to the SA, and with six 4-wire test points.

Current Calculations:

Detector bias will drop $\sim 1\mu\text{V}$ across a $\sim 1\text{m}\Omega$ shunt, so if we use a $1\text{k}\Omega$ load resistor, we must produce 1V @ 300K .

Dissipation at 2K is about 1mW per column.

1st FB is $\sim 1\mu\text{A}$ and gets a $50\Omega/50\Omega$ termination, so we produce only $\sim 200\mu\text{V}$ and dissipate $\sim \text{nW}$ at 2K .

2nd Bias requires $\sim 100\mu\text{A}$ thru 1Ω with 0.1Ω shunt so $\sim 1\text{mA}$ total.

Assume 50Ω of flex, and we put a $50\Omega/50\Omega$ termination @ 2K , so 200mV range @ 300K . 2K dissipation $400\mu\text{W}/\text{col}$.

2nd FB requires $\sim 10\mu\text{A}$ or so, so we terminate with $50\Omega/1\text{k}\Omega$ at 2K and require 20mV @ 300K . 2K dissipation $4\mu\text{W}/\text{col}$.

3rd Bias requires $\sim 100\mu\text{A}$ and has no termination. Dissipation is $\sim 1\mu\text{W}$ at 2K . Need 10mV @ 300K .

3rd FB requires $\sim 10\mu\text{A}$, so we put a $50\Omega/1\text{k}\Omega$ termination to yield 20mV @ 300K , dissipating $4\mu\text{W}/\text{col}$ at 2K .

The total dissipation at 2K is very roughly $2\text{mW}/\text{column}$, a not insignificant amount.

Notes on components:

The singly-hatched cables are Nb/Ti wires with Cu/Ni cladding, in twisted pairs of $0.003"$ conductors woven by TekData.

The doubly-hatched cables are wires mated to the Nanonics connectors at the factory..

I have chosen Nanonics connectors to keep everything small. The wire count is kept lowest if we use:

65 pin connectors for the 64 address wires

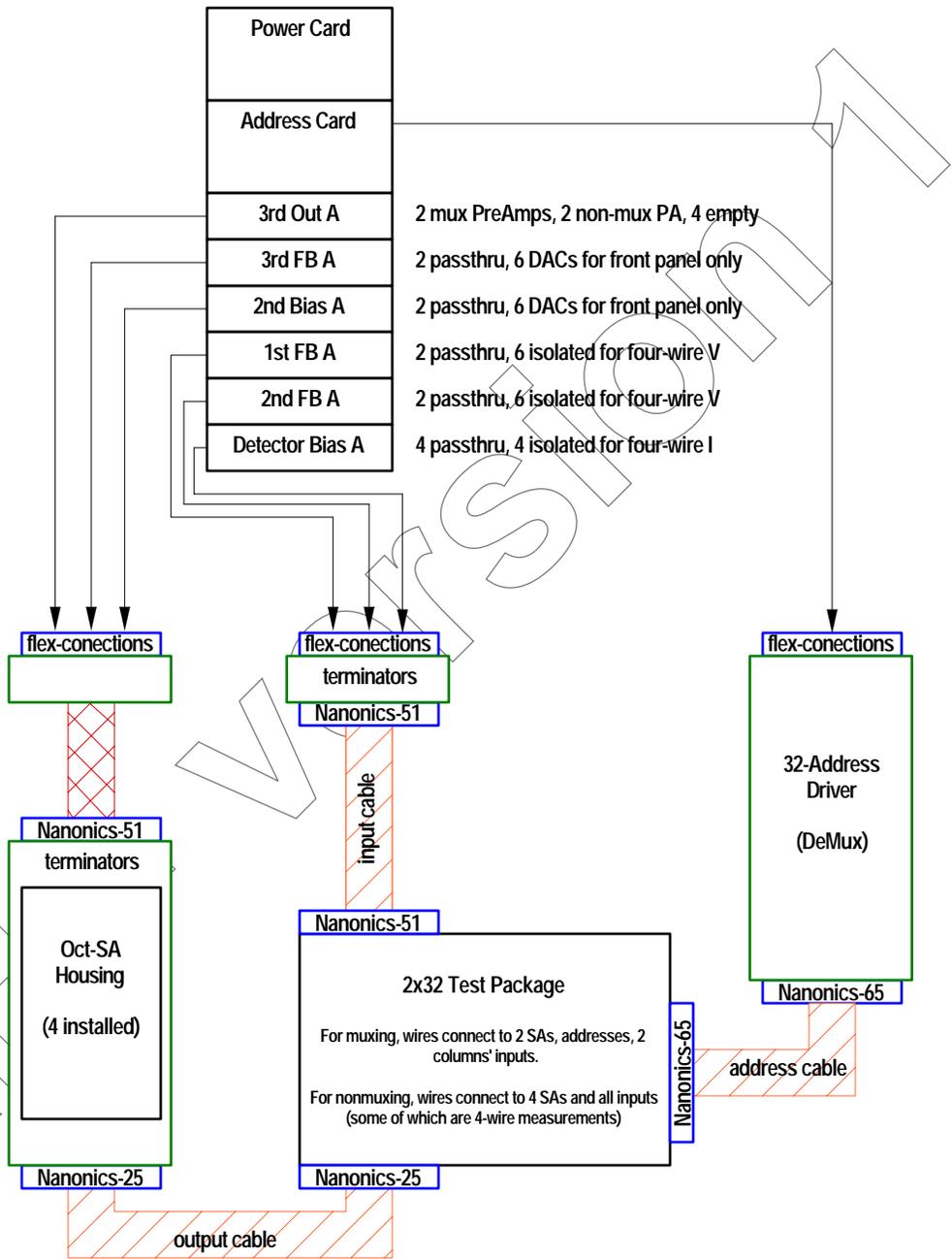
51 pin connectors for the 48 wires to SA and "Inputs"

25 pin connectors for the 16 wires to the "Outputs"

The connection between the SA housing and the Flex lines will be made by buying Nanonics connectors with wires.

These wires will be soldered to the Flex Termination Board.

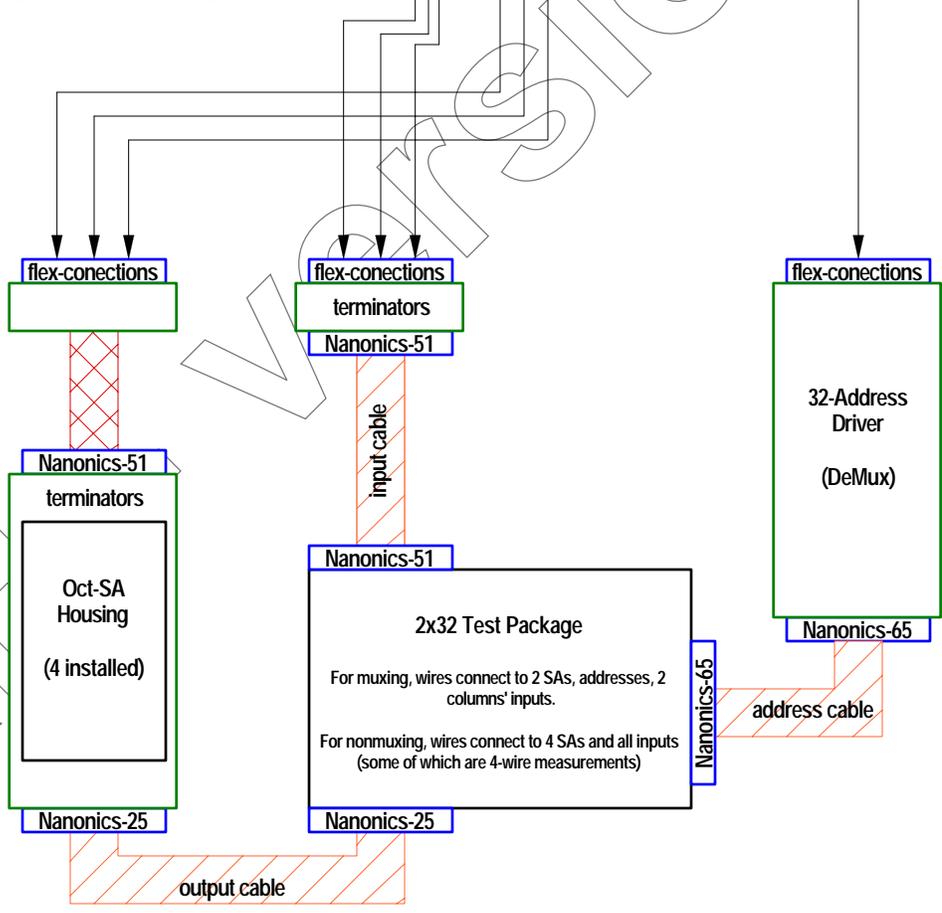
Purple Dewar: 2x32 Test Array Electronics Block Diagram



SAFIRE: 2x32 Array Electronics Block Diagram

-	Power Card	-
-	-	-
-	-	Address Card
-	-	-
-	-	3rd Out A
-	-	3rd FB A
-	-	2nd Bias A
-	-	1st FB A
-	-	2nd FB A
-	-	Detector Bias A

- 2 mux PreAmps, 2 non-mux PA, 4 empty
- 2 passthru, 6 DACs for front panel only
- 2 passthru, 6 DACs for front panel only
- 2 passthru, 6 isolated for four-wire V
- 2 passthru, 6 isolated for four-wire V
- 4 passthru, 4 isolated for four-wire I

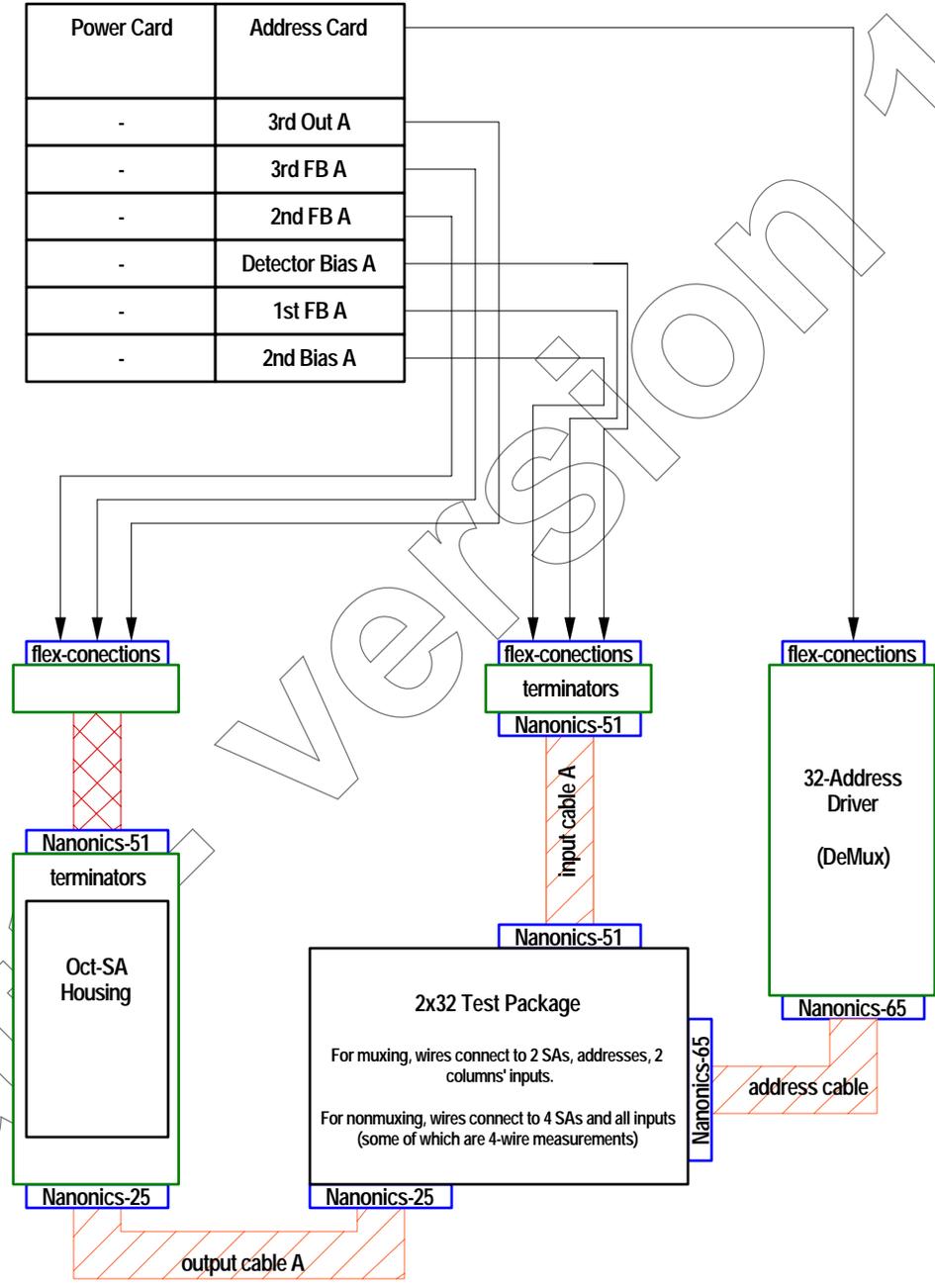


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SPIFI: 2x32 Test Array Electronics Block Diagram

- 2 mux PreAmps, 2 non-mux PA, 4 empty
- 2 passthru, 6 DACs for front panel only
- 2 passthru, 6 DACs for front panel only
- 2 passthru, 6 isolated for four-wire V
- 2 passthru, 6 isolated for four-wire V
- 4 passthru, 4 isolated for four-wire I

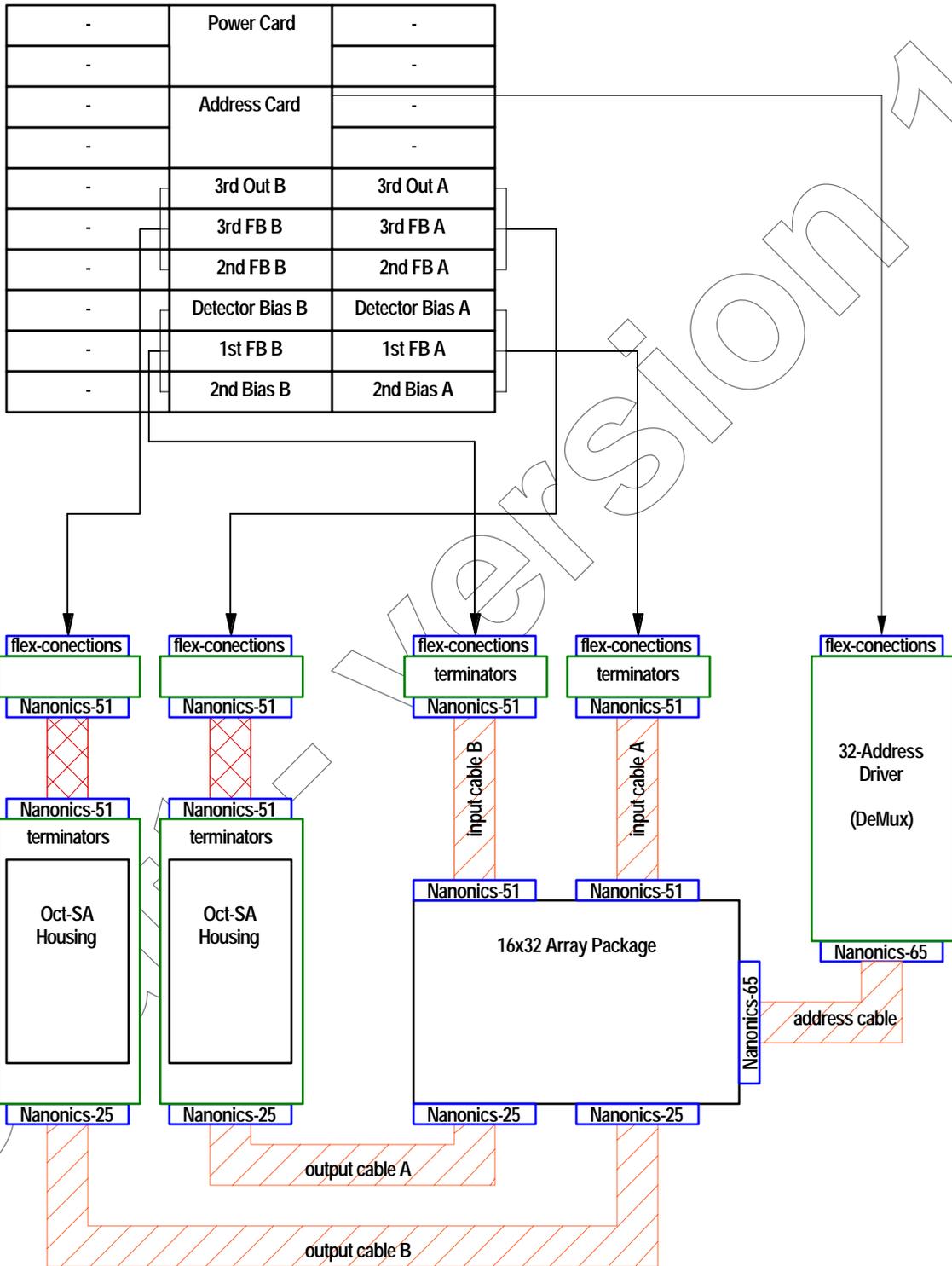
Power Card	Address Card
-	3rd Out A
-	3rd FB A
-	2nd FB A
-	Detector Bias A
-	1st FB A
-	2nd Bias A



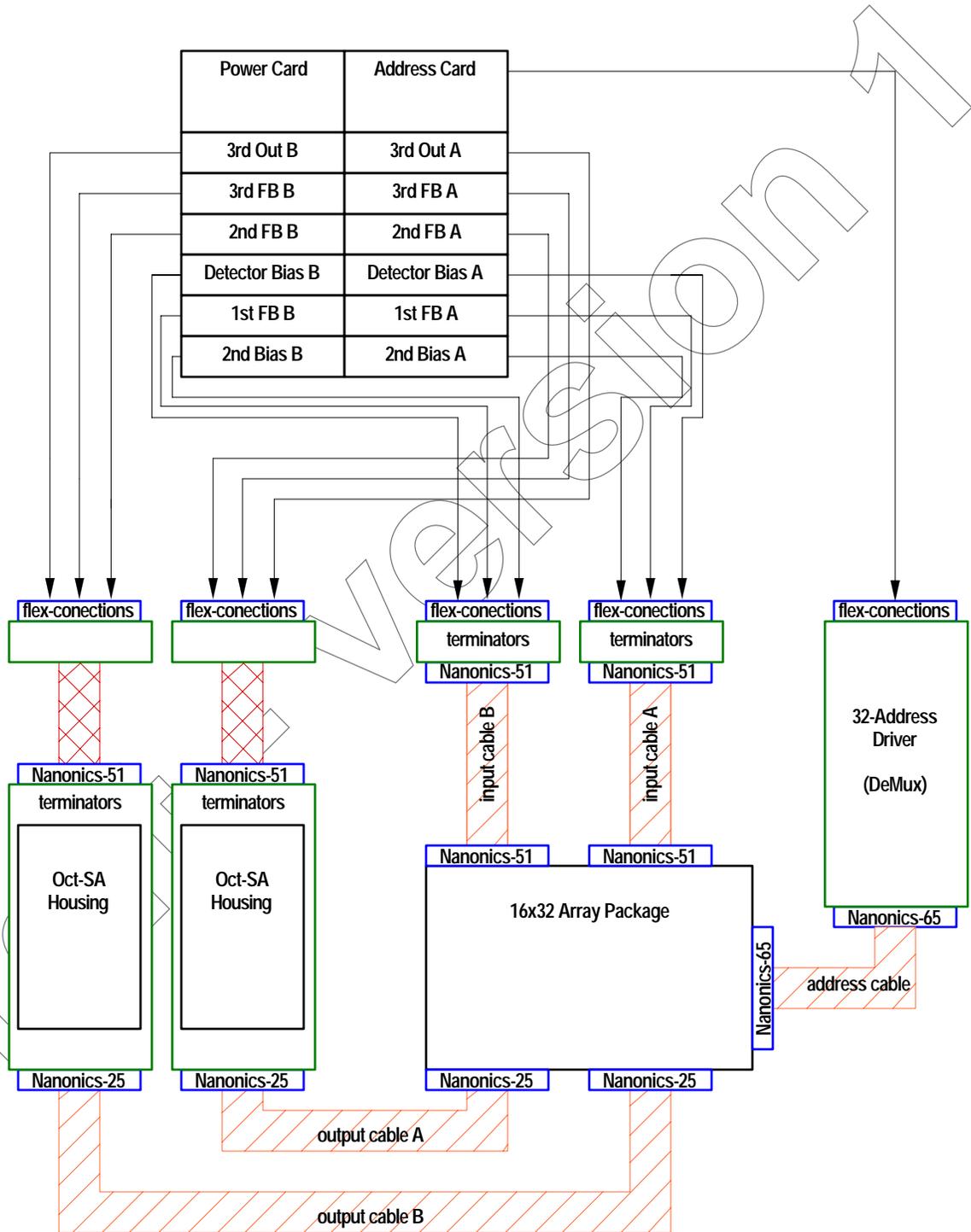
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Version

SAFIRE: 16x32 Array Electronics Block Diagram



SPIFI: 16x32 Array Electronics Block Diagram



SAFIRE: 32x32 Array Electronics Block Diagram

